National Semiconductor

INS8250, INS8250-B Universal Asynchronous Receiver/Transmitter

General Description

Each of these parts function as a serial data input/output interface in a microcomputer system. The system software determines the functional configuration of the UART via a TRI-STATE* 8-bit bidirectional data bus.

The UART performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART. Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt).

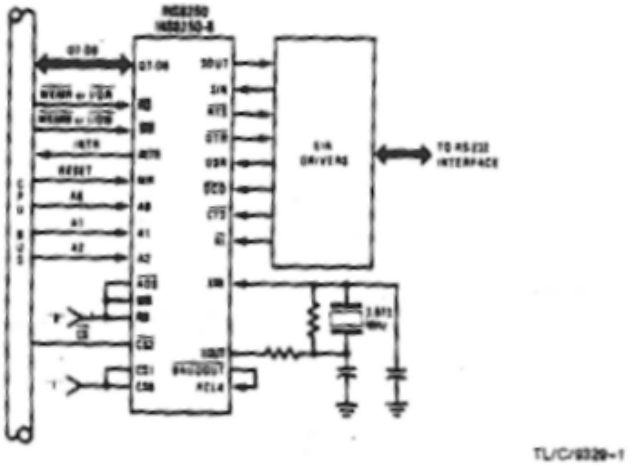
The UART includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to (2^{16}-1), and producing a 16 x clock for driving the internal transmitter logic. Provisions are also included to use this 16 x clock to drive the receiver logic. The UART includes a complete MODEM-control capability and a processor-interrupt system. Interrupts can be programmed to the user's requirements minimizing the computing required to handle the communications link.

National's INS8250 universal asynchronous receiver transmitter (UART) is the unanimous choice of almost every PC and add-on manufacturer in the world. The INS8250 is a programmable communications chip available in a standard 40-pin dual-in-line and a 44-pin PCC package. The chip is fabricated using N-channel silicon gate technology.

Features

Easily interfaces to most popular microprocessors.
Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from serial data stream.
Holding and shift registers eliminate the need for precise synchronization between the CPU and the serial data.
Independently controlled transmit, receive, line status, and data set interrupts.
Programmable baud generator allows division of any input clock by 1 to (2^{16} - 1) and generates the internal 16 x clock.
Independent receiver clock input.
MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD).
Fully programmable serial-interface characteristics:
-- 5-, 6-, 7-, or 8-bit characters
-- Even, odd, or no-parity bit generation and detection
-- 1-, 1½-, or 2-stop bit generation
-- Baud generation (DC to 56k baud).
False start bit detection.
Complete status reporting capabilities.
TRI-STATE TTL drive capabilities for bidirectional data bus and control bus.
Line break generation and detection.
Internal diagnostic capabilities:
-- Loopback controls for communications link fault isolation
-- Break, parity, overrun, framing error simulation.
Fully prioritized interrupt system controls.

Connection Diagram



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1.0 Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	0°C to + 70°C
Storage Temperature	-65°C to + 150°C
All Input or Output Voltages with Respect to Vss	-0.5V to + 7.0V
Power Dissipation	400 mW

Note: *Maximum ratings indicate limits beyond which permanent damage may occur. Continous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics.*

2.0 DC Electrical Characteristics

T_A = 0°C to + 70°C, V_{CC} = +5V =5%, V_{SS} = 0V, unless otherwise specified.

Symbol	Parameter	Conditions	INS8250		INS8250=B		Units
			Min	Max	Min	Max	
V_{ILX}	Clock Input Low Voltage		-0.5	0.8	-0.5	0.8	V
V_{IHX}	Clock Input High Voltage		2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input Low Voltage		-0.5	0.8	-0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}	2.0	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA on all (Note 1)		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0 mA (Note 1)	2.4		2.4		V
I_{CC}(AV)	Avg. Power Supply Current (V_{CC})	V_{CC} = 5.25V, T_A = 25°C No Loads on output SIN, DSR, DCD, CTS, RI = 2.4V All other inputs = 0.4V		80		80	mA
I_L	Input Leakage	V_{CC} = 5.25V, V_{SS} = 0V All other pins floating. V_{IN} = 0V, 5.25V		± 10		± 10	µA
I_{CL}	Clock Leakage			± 10		± 10	µA
I_{OZ}	TRI-STATE Leakage	V_{CC} = 5.25V, V_{SS} = 0V V_{OUT} = 0V, 5.25V 1) Chip deselected 2) WRITE mode, chip selected		± 20		± 20	µA

Capacitance T_A = 25°C, V_{CC} = V_{SS} - 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{XIN}	Clock Input Capacitance	f_c = 1 MHZ Unmeasured pins returned to V_{SS}		15	20	pF
C_{XOUT}	Clock Output Capacitance			20	30	pF
C_{IN}	Input Capacitance			6	10	pF
C_{OUT}	Output Capacitance			10	20	pF

Note 1: Does not apply to XOUT.

3.0 AC Electrical Characteristics T_A = 0°C to + 70°C V_{CC} = + 5V ± 5%

Symbol	Parameter	Conditions	INS8250		INS8250=B		Units
			Min	Max	Min	Max	
t_{ADS}	Address Strobe Width		90		120		ns
t_{AH}	Address Hold Time		0		60		ns
t_{AR}	RD/RD Delay from Address	(Note 1)	110		110		ns
t_{AS}	Address Setup Time		110		110		ns
t_{CH}	Chip Select Hold Time		0		60		ns
t_{CS}	Chip Select Setup Time		110		110		ns
t_{CSC}	Chip Select Output Delay from Select	@ 100 pF loading (Note 1)		200		200	ns
t_{CSR}	RD/RD Delay from Chip Select	(Note 1)	110		110		ns
t_{CSS}	Chip Select Output Delay from Strobe		0	150	0	150	ns
t_{CSW}	WR/WR Delay from Select	(Note 1)	160		160		ns
t_{CH}	Data Hold Time		60		100		ns
t_{DS}	Data Setup Time		175		350		ns
t_{HZ}	RD/RD to Floating Data Delay	@ 100 pF loading (Note 3)	0	150	0	150	ns
t_{MR}	Master Reset Pulse Width		10		10		µs
t_{RA}	Address Hold Time from RD/RD	(Note 1)	50		50		ns
t_{RC}	Read Cycle Delay		1735		1735		ns
t_{RCS}	Chip Select Hold Time from RD/RD	(Note 1)	50		50		ns
t_{RD}	RD/RD Strobe Width		175		350		ns
t_{RDA}	Read Strobe Delay		0		0		ns
t_{RDD}	RD/RD to Driver Disable Delay	@ 100 pF loading (Note 3)		150		250	ns
t_{RVD}	Delay from RD/RD to Data	@ 100 pF loading		250		300	ns
t_{WA}	Address Hold Time from WR/WR	(Note 1)	50		50		ns
t_{WC}	Write Cycle Delay		1785		1785		ns
t_{WCS}	Chip Select Hold Time from WR/WR	(Note 1)	50		50		ns
t_{WDA}	Write Strobe Delay		50		50		ns
t_{WR}	WR/WR Strobe Width		175		350		ns
t_{XH}	Duration of Clock High Pulse	External Clock (3.1 MHz Max.)	140		140		ns
t_{XL}	Duration of Clock Low Pulse	External Clock (3.1 MHz Max.)	140		140		ns
t_{RC}	Read Cycle = $t_{AR} + t_{DIW} + t_{RC}$		2000		2205		ns
t_{WC}	Write Cycle = $t_{DDA} + t_{DDW} + t_{WC}$		2100		2305		ns
Baud Generator							
N	Baud Divisor		1	$2^{16} - 1$	1	$2^{16} - 1$	
t_{BHD}	Baud Output Positive Edge Delay	100 pF Load		250		250	ns
		100 pF Load					
		f_x = 3 MHz, ÷ 3, 100 pF Load	330		330		ns
		f_x = 2 MHz, ÷ 2, 100 pF Load	425		425		ns
Receiver							
t_{RINT}	Delay from RD/RD (RD RBR or RD LSR) to Reset Interrupt	100 pF Load		1000		1000	ns
t_{SCD}	Delay from RCLK to Sample Time			2000		2000	ns
t_{SINT}	Delay from Stop to Set Interrupt			2000		2000	ns

Note 1: Appricable only when ADS is tied low.

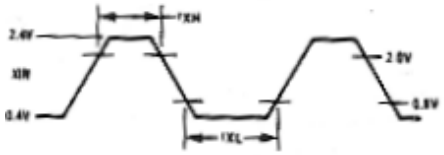
Note 2: Charge and discharge time as determined by V_{CD} V_{OH} and the external loading.

3.0 AC Electrical Characteristics T_A = 0°C to + 70°C V_{CC} = + 5V ± 5% (Continued)

Symbol	Parameter	Conditions	INS8250		INS82C50=B		Units
			Min	Max	Min	Max	
Transmitter							ns
HR	Delay from RD/RD (RD HR) to Reset Interrupt (THRE)	100 pF Load		1000		1000	ns
4_{AS}	Delay from Initial INTR Reset to Transmit Start			16		16	BAUDOUT Cycles
I_{SI}	Delay from Initial Write to Interrupt			50		50	BAUDOUT Cycles
I_{SS}	Delay from Stop to Next Start			1000		1000	ns
ISTI	Delay from Stop to Interrupt (THRE)			8		8	BAUDOUT Cycles
Modem Control							
I_{MDO}	Delay from WR/WR (WR MCR) to Output	100 pF Load		1000		1000	ns
I_{PIM}	Delay to Reset Interrupt from RD/RD (RD MSR)	100 pF Load		1000		1000	ns
I_{SIM}	Delay to Set Interrupt from MODEM Input	100 pF Load		1000		1000	ns

4.0 Timing Waveforms (All timings are referenced to valid 0 and valid 1)

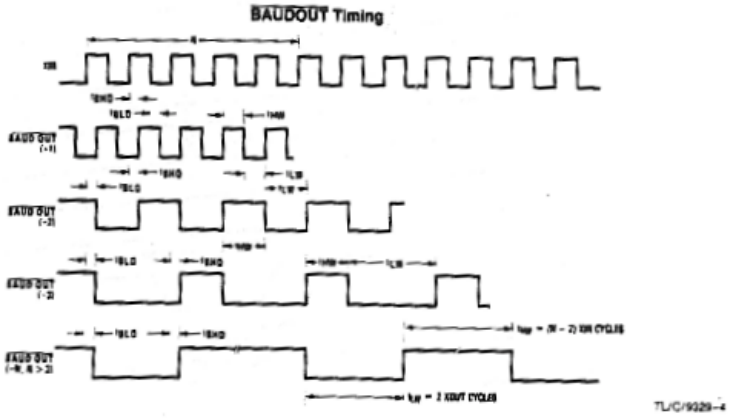
External Clock Input (3.1 MHz Max.)



AC Teat Points

Note 1: The 2.4V and 0.4V levels are the voltages that the inputs are driven to during AC testing.
Note 2: The 2.0V and 0.8V levels are the voltages at which the timing tests are made.

BAUDOUT Timing



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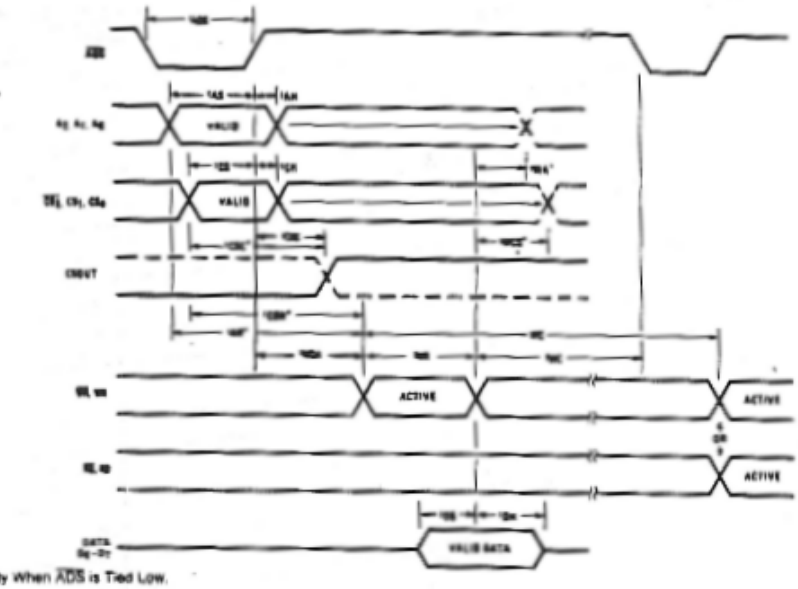
4.0 Timing Waveforms (Continued)

Write Cycle



*Applicable Only When $\overline{ADS}$ is Tied Low.

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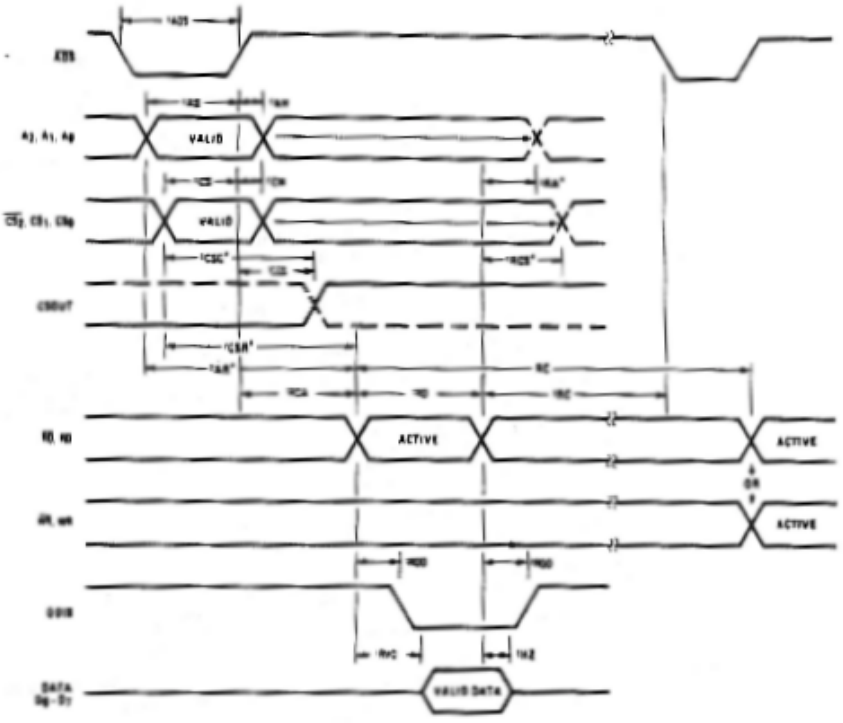
Read Cycle



*Applicable Only When $\overline{ADS}$ is Tied Low.

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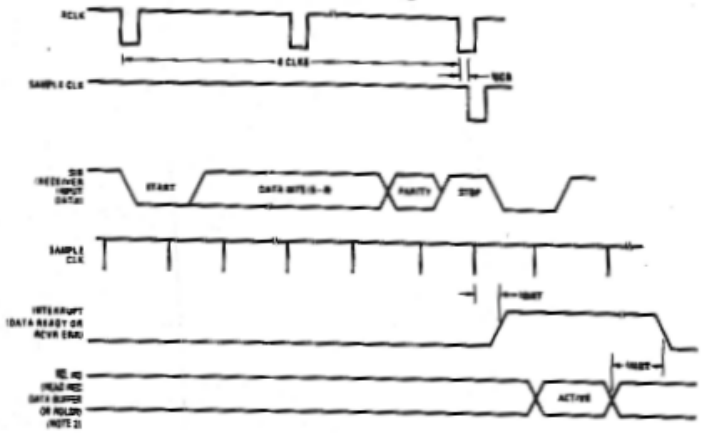
4.0 Timing Waveforms (Continued)

Receiver Timing



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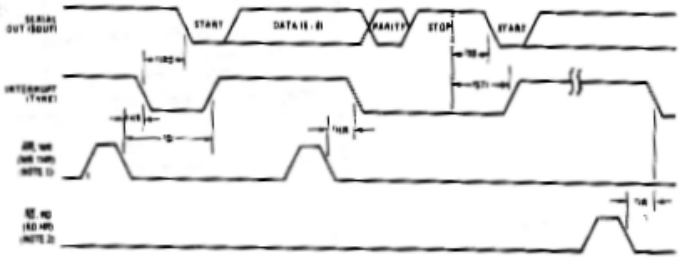
Transmitter Timing



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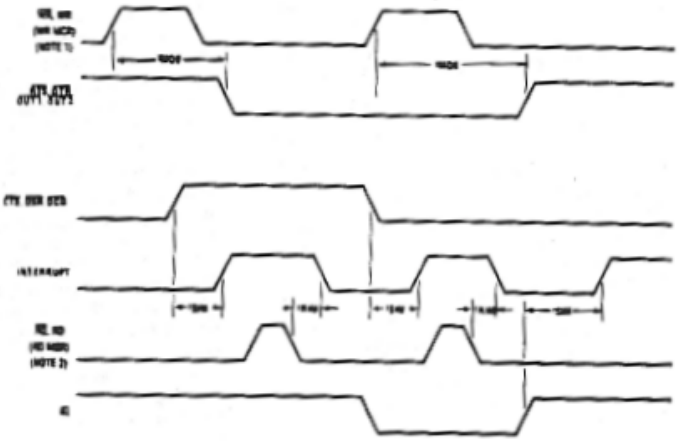
MODEM Controls Timing



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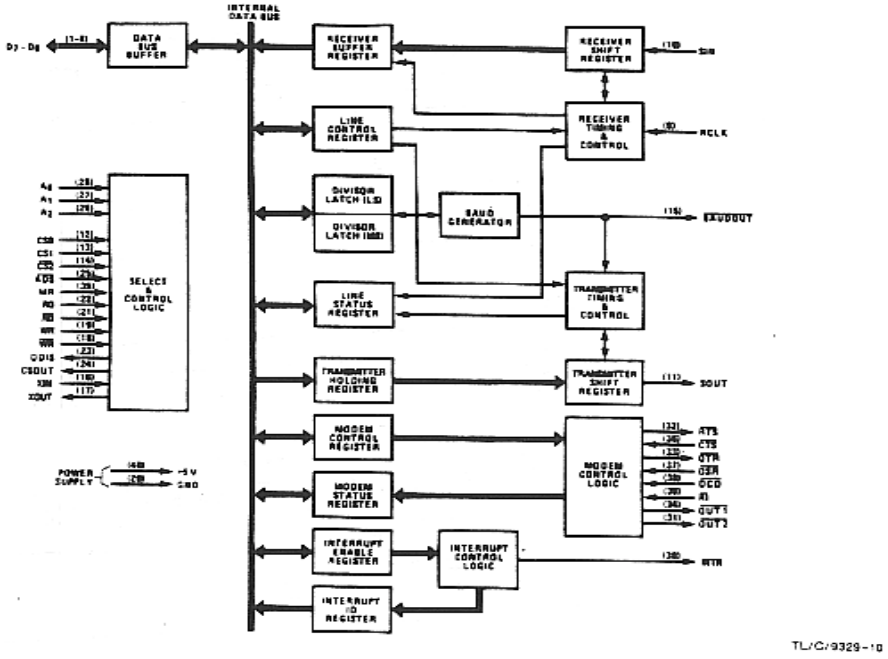
Note 1: See Write Cycle Timing

Note 2: See Read Cycle Timing

5.0 Block Diagram



Note: Applicable pinout numbers are included within parenthesis.

6.0 Pin Descriptions

The following describes the function of all UART, pins. Some of these descriptions reference internal circuits.

In the following descriptions, a low represents a logic 0 (0V nominal) and a high represents a logic 1 (+ 2.4V nominal).

6.1 INPUT SIGNALS

Chip Select (CS0, CS1, CS2), Pins 12-14: When CSO and CS1 are high and CS2 is low, the chip is selected. This enables communication between the UART and the CPU. The positive edge of an active Address Strobe signal latches the decoded chip select signals, completing chip selection. If ADS is always low valid chip selects should stabilize according to the CSW parameter.

Read (RD, RD), Pins 22 and 21: When RD is high or RD is low while the chip is selected, the CPU can read status information or data from the selected UART register.

Note: Only an active RD or RD input is required to transfer data from the UART during a read operation. Therefore, the either the RD input permanently low of the RD input permanently high, when it is not used.

Write (WR, WR), Pins 19 and 18: When WR is high or WR is low while the chip is selected, the CPU can write control words or data into the selected UART register.

Note: Only an active WR or WR input is required to transfer data to the UART during a write operation. Therefore, the either the WR input permanantly low or the WR input permanently high, when it is not used.

Address Strobe (ADS), Pin 25: The positive edge of an active Address Strobe (ADS) signal latches the Register Select (A0, A1, A2) and Chip Select (CS0, CS1, CS2) signals.

Note: An active ADS input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, be the ADS input permanently low.

Register Select (A0, A1, A2), Pins 26-2B: Address signals connected to these 3 inputs select a UART register for the CPU to read from or write to during data transfer. A table of registers and their addresses is shown below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain UART registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

DLAB	A_2	A_1	A_0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

Register Addresses

Master Reset (MR), Pin 35: When this input is high, it clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the UART. The states of various output signals (SOUT, INTR, OUT 1, OUT 2, RTS, DTR) are affected by an active MR input. (Refer to Table 1.).

Receiver Clock (RCLK), Pin 9: This input is the 16 x baud rate clock for the receiver section of the chip.

Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, MODEM, or data set).

Clear to Send (CTS), Pin 36: When low, this indicates that the MODEM or data set is ready to exchange data. The CTS signal is a MODEM status input whose conditions can be tested by the CPU reading bit 4 (CTS) of the MODEM Status Register. Bit 4 is the complement of the CTS signal. Bit 0 (DCTS) of the MODEM Status Register indicates whether the CTS input has changed state since the previous reading of the MODEM Status Register. CTS has no effect on the Transmitter.

Note: Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status interrupt is enabled.

Data Set Ready (DSR), Pin 37: When low, this indicates that the MODEM or data set is ready to establish the communications link with the UART. The DSR signal is a MODEM status input whose condition can be tested by the CPU reading bit 5 (DSR) of the MODEM Status Register. Bit 5 is the complement of the DSR Signal. Bit 1 (DDSR) of the MODEM Status Register indicates whether the DSR input has changed state since the previous reading of the MODEM Status Register.

Note: Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status interrupt is enabled.

Data Carrier Detect (DCD), Pin 38: When low, indicates that the data carrier has been detected by the MODEM or data set. The DCD signal is a MODEM status input whose condition can be tested by the CPU reading bit 7 (DCD) of the MODEM Status Register. Bit 7 is the complement of the DCD signal. Bit 3 (DDCD) of the MODEM Status Register indicates whether the DCD input has changed state since the previous reading of the MODEM Status Register. DCD has no effect on the receiver.

Note: Whenever the DCD bit of the MODEM Status Register changes state, an interrupt is generated of the MODEM Status Interrupt is enabled.

Ring Indicator (RI), Pin 39: When low, this indicates that a telephone ringing signal has been received by the MODEM or data set. The RI signal is a MODEM status input whose condition can be tested by the CPU reading bit 6 (RI) of the MODEM Status Register. Bit 6 is the complement of the RI signal. Bit 2 (TERI) of the MODEM Status Register indicates whether the RI input signal has changed from a low to a high state since the previous reading of the MODEM Status Register.

Note: Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status Interrupt is enabled.

V_{CC1} Pin 40: + 5V supply.
V_{SS1} Pin 20: Ground (OV) reference.

6.2 OUTPUT SIGNALS

Data Terminal Ready (DTR), Pin 33: When low, this informs the MODEM or data set that the UART is ready to establish a communications link. The DTR output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state.

Request to Send (RTS), Pin 32: When low, this informs the MODEM or data set that the UART is ready to exchange data. The RTS output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. A Master Reset operation sets this signal to its inactive (high) state.

Output 1 (OUT 1), Pin 34: This user-designated output can be set to an active low by programming bit 2 (OUT 1) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. In the XMOS parts this will achieve TTL levels.

Output 2 (OUT 2), Pin 31: This user-designated output can be set to an active low by programming bit 2 (OUT 1) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. In the XMOS parts this will achieve TTL levels.

Chip Select Out (CSOUT), Pin 24: When high, it indicates that the chip has been selected by active. CS0, CS1, and CS2 inputs. No data transfer can be initiated until the CSOUT signal is a logic 1. CSOUT goes low when the UART is deselected.

Driver Disable (DDIS), Pin 23: This goes low whenever the CPU is reading data from the UART. It can disable or control the direction of a data bus transceiver between the CPU and the UART (see Typical Interface for a High Capacity Data Bus).

Baud Out (BAUDOUT), Pin 15: This is the 16 x clock signal from the transmitter section of the UART. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The BAUDOUT may also be used for the receiver section by tying this output to the RCLK input of the chip.

6.0 Pin Descriptions (Continued)

Interrupt (INTR), Pin 30: This goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Line Status; Received Data Available; Transmitter Holding Register Empty: and MODEM Status. The INTR signal is reset low upon the appropriate interrupt service or a Master Reset operation.

Serial Output (SOUT), Pin 11: This is the composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation or when the transmitter is idle.

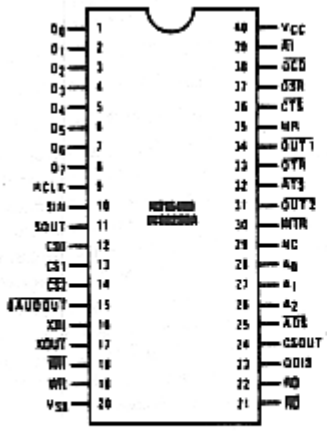
6.3INPUT/OUTPUT SIGNALS

Data (D7-D0) Bus, Pins 1-8: This bus is comprised of eight TRI-STATE input/output lines. The bus provides bidlrectional communications between the UART and the CPU. Data control words, and status information are transferred via the D_7-D_0 Data Bus.

External Clock Input/Output (X_{IN}, X_{OUT}) Pins 16 and 17: These two pins connect the main timing reference (crystal or signal clock) to the UART. When a crystal oscillator or a clock signal is provided, it drives the UART via XIN (see typical oscillator network illustration).

7.0 Connection Diagrams

Dual-In-Line Package



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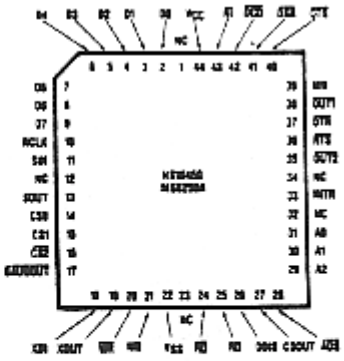
Top View

Order Number INS8250N, INS8250N-B or INS8250N/A+
See NS Package Number N40A

PCC Package



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Top View

Order Number INS8250V-B
See NS Package Number V44A

TABLE 1, UART Reset Functions

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	**0000** 0000 (Note 1)
Interrupt Identification Register	Master Reset	**00000** 001
Line Control Register	Master Reset	0000 0000
MODEM Control Register	Master Reset	**0000** 0000
Line Status Register	Master Reset	**0**110 0000
MODEM Status Register	Master Reset	XXXX 0000 (Note 2)
SOUT	Master Reset	High
INTR (RCVR Errs)	Read LSR/MR	Low
INTR (RCVR Data Ready)	Read RBR/MR	Low
INTR (THRE)	Read IIR/Write THR/MR	Low
INTR (Modem Status Changes)	Read MSR/MR	Low
OUT 2	Master Reset	High
RTS	Master Reset	High
DTR	Master Reset	High
OUT 1	Master Reset	High

Note 1: Underlined bits are permanently low.
Note 2: Bits 7-4 are driven by the input signals.

8.0 Registers

The system programmer may access any of the UART registers summarized in Table If via the CPU. These registers control UART operations including transmission and reception of data. Each register bit in Table II has its name and reset state shown.

8.1 LINE CONTROL REGISTER

The system programmer specifies the format of the asynchronous data communications exchange and sets the Divisor Latch Access bit via the Line Control Register (LCR). The programmer can also read the contents of the Line Control Register. The read capability simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. Table II shows the contents of the LOR. Details on each bit follow:

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Character Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits transmitted and received in each serial character. If bit 2 is a logic 0, one Stop bit is generated or checked in the serial data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0.

TABLE II. Summary of Registers

Bill No.	Register Address									
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	3	4	5	6	0 DLAB = 1	1 DLAB = 1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident Register (Read Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Divisor Latch (LS)	Division Latch (MS)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	DLL	DLM
0	Data Bit 0 (Note 1)	Data Bit 0	Received Data Available	" 0" if Interrupt Pending	Word Length Select Bit 0 (WLSO)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta 0 Clear to Send (DCTS)	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Transmitter Holding Register Empty	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Receiver Line Status	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	MODEM Status	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Shift Register Empty (TSRE)	Ring Indicator (RI)	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Data Carrier Detect (DCD)	Bit 7	Bit 15

Note 1: Bit 0 is the least significant bit, it is the first bit serially transmitted or received.

8.0 Registers (Continued)

and 1, one and a half Stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bits are generated. The Receiver checks the first Stop bit only, regardless of the number of Stop bits selected.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of is when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bits 3, 4 and 5 are logic 1 the Parity bit is transmitted and checked as a logic 0. If bits 3 and 5 are 1 and bit 4 is a logic 0 then the Parity bit is transmitted and checked as a logic 1. If bit 5 is a logic 0 Stick Parity is disabled.

Bit 6: This bit is the Break Control bit. It causes a break condition to be transmitted by the UART. When it is set to a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by clearing bit 6 to a logic 0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic.

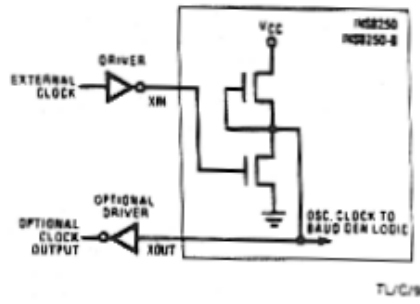
Note: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is used no erroneous or extraneous characters was be transmitted because of the break.

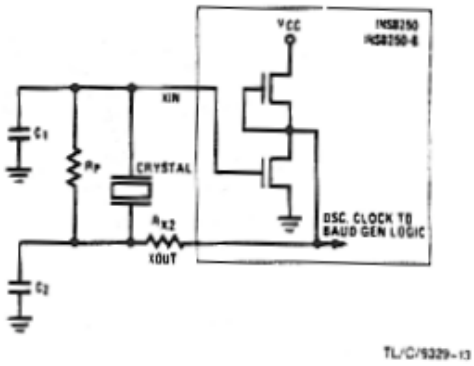
1. Load an all Us, pad character, in response to THRE.
2. Set break alter the next THRE.
3. Wait for the transmitter to be idle. (TSRE-1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

8.2 Typical Clock Circuits





Typical Oscillator Networks

Crystal	R_P	R_{x2}	C_1	C_2
1.8-3.1 MHz	1 MΩ	1.5k	10-30 pF	40-60 pF

TABLE III. Baud Rates Using 1.8432 MHz Crystal

Desired Baud Rate	Decimal Divisor Used to Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	2304	-
75	1538	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	98	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.86

TABLE IV. Baud Rates Using 3.072 MHz Crystal

Desired Baud Rate	Decimal Divisor Used to Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	3840	-
75	2560	-
110	1745	0.026
134.5	1428	0.034
150	1280	-
300	640	-
600	320	-
1200	160	-
1800	107	0.312
2000	96	-
2400	80	-
3600	53	0.828
4800	40	-
7200	27	1.23
9600	20	-
19200	10	-
38400	5	-

8.3 PROGRAMMABLE BAUD GENERATOR

The UART contains a programmable Baud Generator that is capable of taking any clock input from DC to 3.1 MHz and dividing it by any divisor from 1 to 2^{18}-1. The output frequency of the Baud Generator is 16 x the Baud [divisor ? ? - (frequency input)[baud rate x 16)] . Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure proper operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded.

Tables III and IV provide decimal divisors to use with crystal frequencies of 1.8432 MHz and 3.072 MHz, respectively, for common baud rates. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. Using a division of D is not recommended.

Note: The maximum operating frequency of the Baud Generator is 3.1 MHz However, when using divisors of 3 and below, the maximum frequency is equal to the divisor in MHz. For example, if the divisor is 1, then the maximum frequency is 1 MHz. In no case should the data rate be greater than 56k Baud.

8.4 LINE STATUS REGISTER

This 8-bit register provides status information to the CPU concerning the data transfer. Table if shows the contents of the Line Status Register. Details on each bit follow:

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 is reset to a logic 0 by reading the data in the Receiver Buffer Register.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is set to a logic 1 upon detection of an overrun condition and reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or panty bit is a logic 0 (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status Register. The UART will try to resynchronize after a framing error. To do this it assumes that the framing error was due to the next start bit, so it samples this " start" bit twice and then takes in th " data" .

Bit 4: This bit is the Break interrupt (B1) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The B1 indicator is reset whenever the CPU reads the contents of the Line Status Register. Restarting after a break is received, requires the SIN pin to be logical 1 for at least 1/2 bit time.

Note: Bits 1 through 4 are the error conditions that produce a Recover Line Status interrupt whenever any of the corresponding conditions are detached and the interrupt is enabled.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 whenever the CPU loads the Transmitter Holding Register.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register (TSR) is empty. It is reset to a logic 0 whenever a data character is transferred to the TSR.

Bit 7: This bit is permanently set to logic 0.

Note: The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing.

TABLE V. Interrupt Control Functions

Interrupt Identification Register				Interrupt Set and Reset Functions		
Bit 2	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	1	-	None	None	-
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

8.5 INTERRUPT IDENTIFICATION REGISTER

In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the interrupt identification Register. The four levels of interrupt conditions in order of priority are Receiver Line Status: Received Data Ready: Transmitter Holding Register Empty; and MODEM Status.

When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occuring, the UART records new interrupts, but does not change its current indication until the access is complete, Table II shows the contents of the IIR. Details on each bit follow:

Bit 0: This bit can be used in an interrupt environment to indicate whether an interrupt condition is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table V.

Bits 3 through 7: These five bits of the IIR are always logic 0.

8.6 INTERRUPT ENABLE REGISTER

This register enables the four types of UART interrupts. Each interrupt can individually activate the interrupt (INTR) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the interrupt Enable Register (IER). Similarly, setting bits of this register to a logic 1, enables the selected interrupt(s). Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the INTR output signal. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. Table it shows the contents of the IER. Details on each bit follow.

Bit 0: This bit enables the Received Data Available interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

8.7 MODEM CONTROL REGISTER

This register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register (MCR) are indicated in Table II and are described below. Table II shows the contents of the MCR. Details on each bit follow.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

Note: The $\overline{DTR}$ output of the DART may be applied to an ELA inverting the driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\ 1}$) signal, which is an auxillary user-designated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occur; the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is " looped back" into the Receiver Shift Register input, the four MODEM Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, and $\overline{DCD}$) are disconnected; and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four MODEM Control inputs. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit-and received-data paths of the UART.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control interrupts are also operational, but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the interrupt Enable Register.

Bits 5 through 7: These bits are permanently set to logic 0.

8.8 MODEM STATUS REGISTER

This register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

Table II shows the contents of the MSR. Details on each bit follow:

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state.

Bit 3: This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status interrupt is generated.

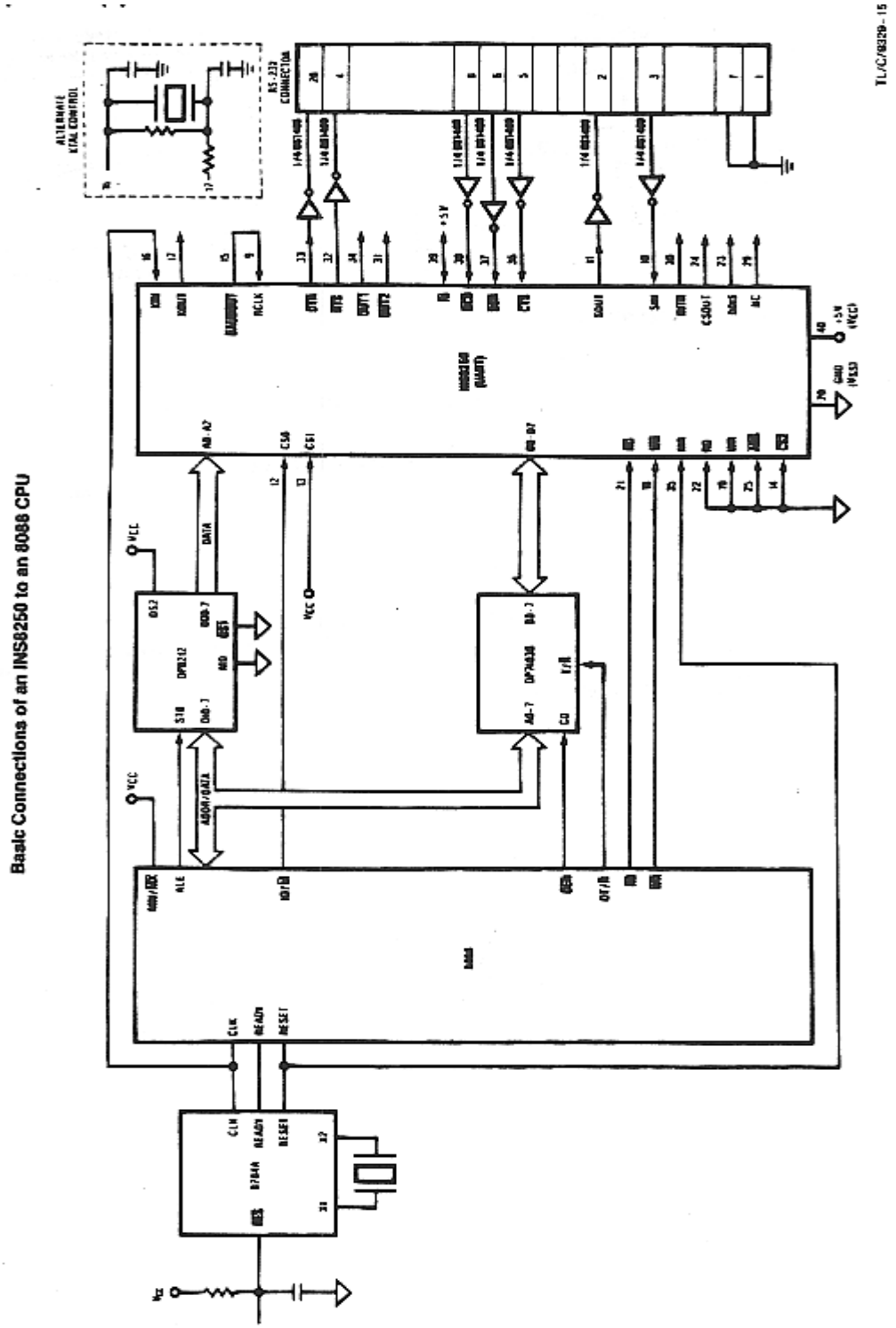
Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. It bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) Input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator. ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 in the MCR.

9.0 Typical Applications

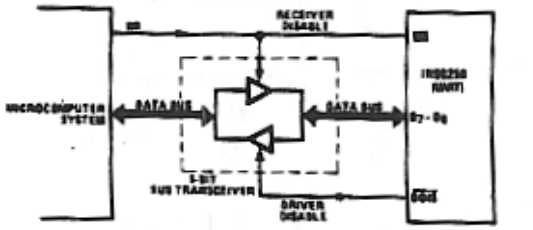


Basic Connections of an INS8250 to an 8088 CPU

Jameco Part number 52628

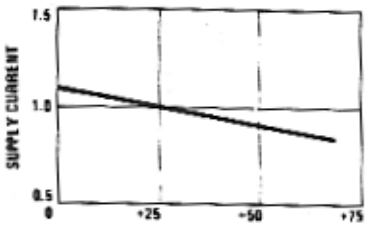
9.0 Typical Applications (Continued)

Typical Interface for a High-Capacity Data Bus



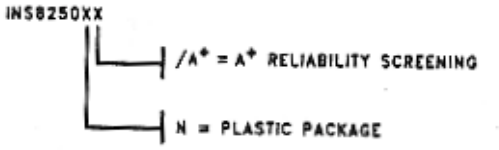
TL/C/9329–16

Typical Supply Current vs Temperature, Normalized



TL/C/9329–17

10.0 Ordering Information



TL/C/9329–19

TL/C/9329–20

11.0 Reliability Information

Gate Count 2,000

Transistor Count 4,500